Abstract

An information processor having a normal-operation mode in which coherence control is performed for making data in a cache memory of a processor identical to data in a main memory and a power-saving mode in which the coherence control is suppressed to lower the power consumption from power consumption in the normal-operation mode and entering the normal-operation mode when an input/output device accesses the main memory in the power-saving mode includes an attribute setting module for setting a device area of the main memory, accessed by the input/output device of the information processor to a non-cacheable attribute for exempting said device area from said coherence control even in the normal-operation mode; an operation mode setting module for allowing the input/output device to access the device area while keeping the operation mode of the information processor in the power-saving mode when the input/output device requests access to the device area in the power-saving mode.